

# SOP-8L Plastic-Encapsulate MOSFETS

## LJ9926NT7G

NCE N-Channel Enhancement Mode Power MOSFET

### Description

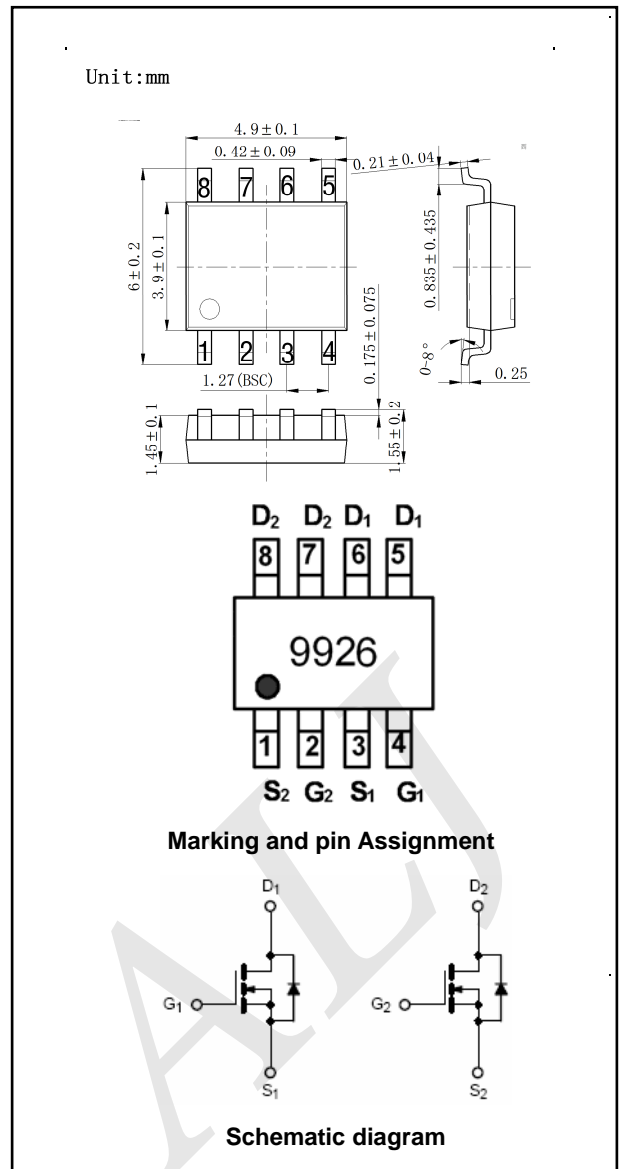
The LJ9926NT7G uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### General Features

- $V_{DS} = 20V, I_D = 6A$   
 $R_{DS(ON)} < 28m\Omega @ V_{GS} = 4.5V$   
 $R_{DS(ON)} < 37m\Omega @ V_{GS} = 2.5V$
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current

### Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
9926	LJ9926NT7G	SOP-8	Ø330mm	12mm	2500 units

### Absolute Maximum Ratings ( $T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
$V_{DS}$	Drain-Source Voltage	20	V
$V_{GS}$	Gate-Source Voltage	±10	V
$I_D$	Drain Current-Continuous	6	A
$I_D(100^\circ C)$	Drain Current-Continuous( $T_C = 100^\circ C$ )	3.8	A
$I_{DM}$	Pulsed Drain Current	25	A
$P_D$	Maximum Power Dissipation	1.25	W
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 To 150	°C

### Thermal Characteristic

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	100	°C/W
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## Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

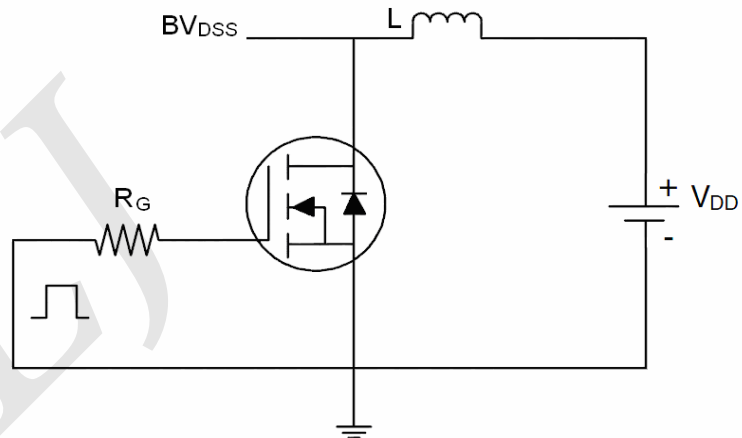
Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	20	22	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V	-	-	1	μA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> =±10V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics</b> (Note 3)						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.5	0.7	1.2	V
R <sub>DS(on)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =4.5V, I <sub>D</sub> =6A	-	20	28	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =5A	-	26	37	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =6A	20	-	-	S
<b>Dynamic Characteristics</b> (Note 4)						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =10V, V <sub>GS</sub> =0V, F=1.0MHz	-	640	-	PF
C <sub>oss</sub>	Output Capacitance		-	140	-	PF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	80	-	PF
<b>Switching Characteristics</b> (Note 4)						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> =10V, I <sub>D</sub> =1A V <sub>GEN</sub> =4.5V, R <sub>G</sub> =6Ω	-	8	-	nS
t <sub>r</sub>	Turn-on Rise Time		-	9	-	nS
t <sub>d(off)</sub>	Turn-Off Delay Time		-	15	-	nS
t <sub>f</sub>	Turn-Off Fall Time		-	4	-	nS
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =10V, I <sub>D</sub> =3A, V <sub>GS</sub> =4.5V	-	10	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	1.5	-	nC
Q <sub>gd</sub>	Gate-Drain Charge		-	1.6	-	nC
<b>Drain-Source Diode Characteristics</b>						
V <sub>SD</sub>	Diode Forward Voltage (Note 3)	V <sub>GS</sub> =0V, I <sub>S</sub> =1.7A	-	-	1.2	V
I <sub>S</sub>	Diode Forward Current (Note 2)		-	-	6	A

### Notes:

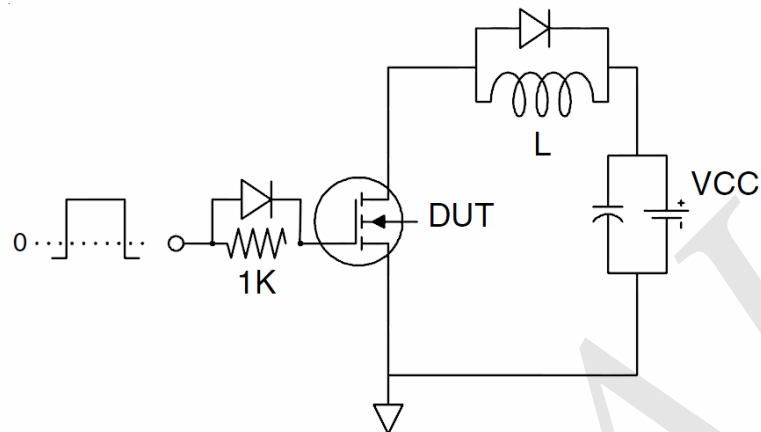
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

## Test Circuit

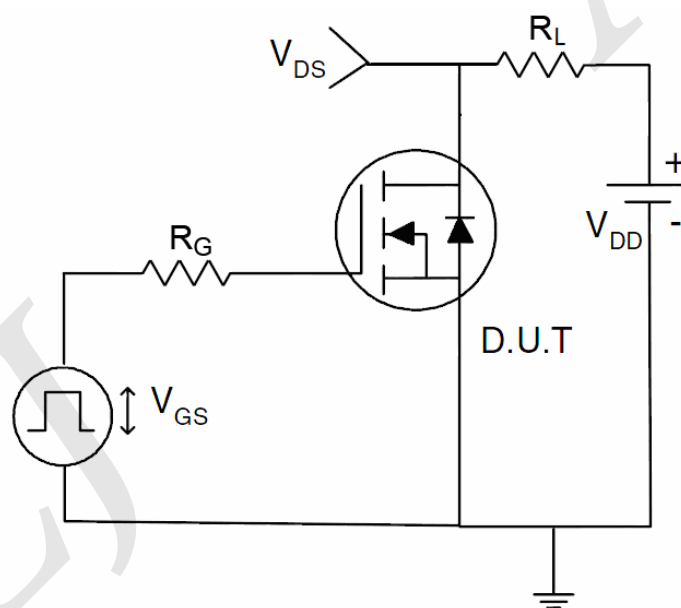
### 1) $E_{AS}$ Test Circuits



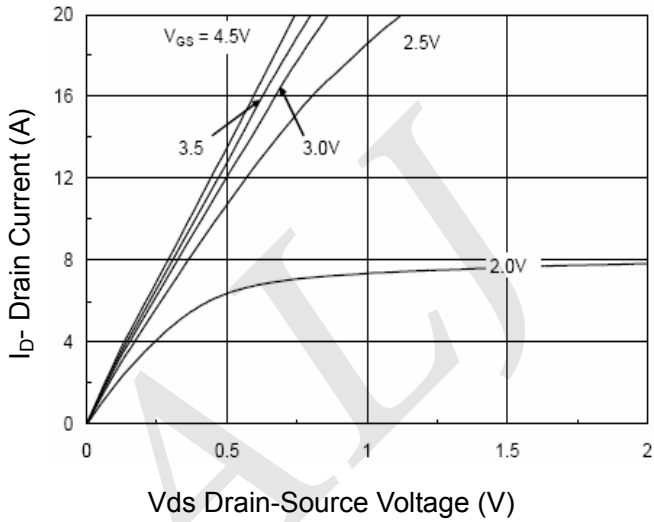
### 2) Gate Charge Test Circuit:



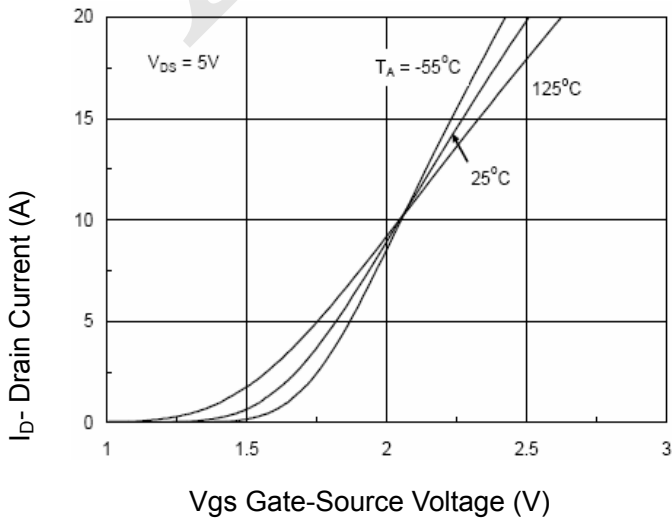
### 3) Switch Time Test Circuit:



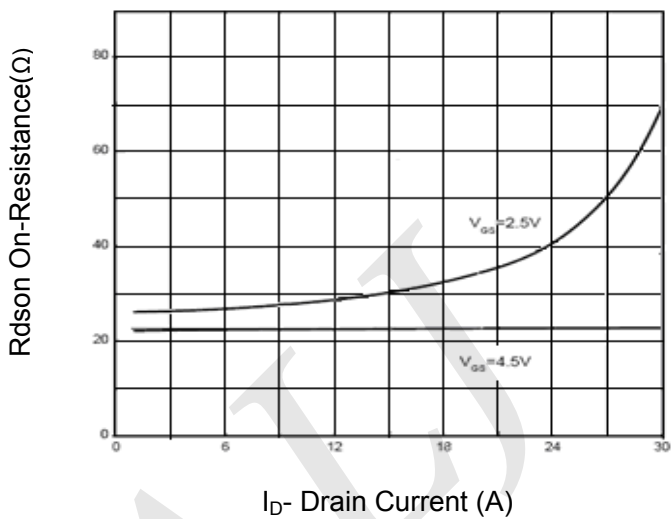
## Typical Electrical and Thermal Characteristics (Curves)



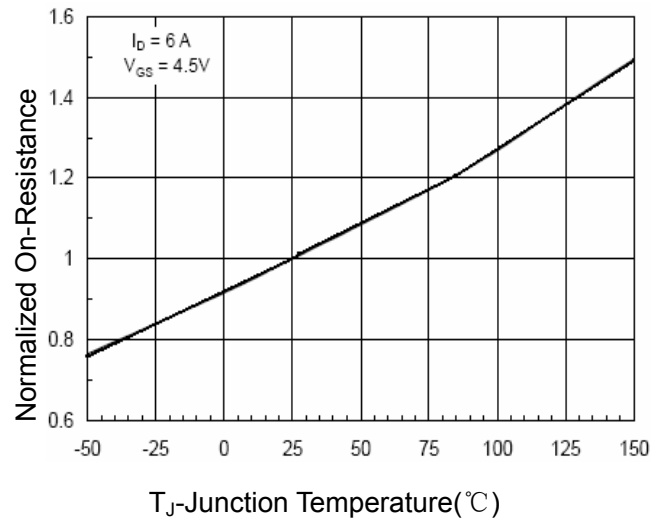
**Figure 1 Output Characteristics**



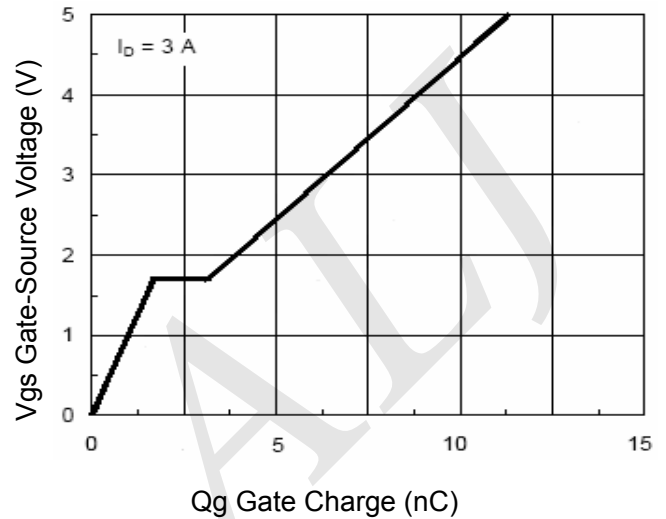
**Figure 2 Transfer Characteristics**



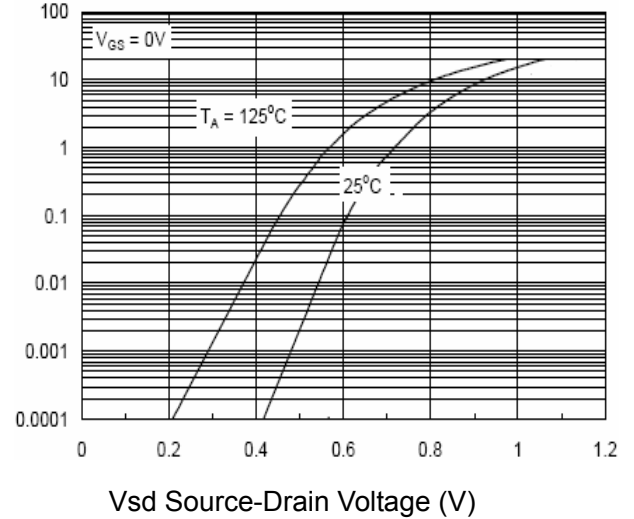
**Figure 3  $R_{DS(on)}$ - Drain Current**



**Figure 4  $R_{DS(on)}$ -Junction Temperature**



**Figure 5 Gate Charge**



**Figure 6 Source- Drain Diode Forward**

## Typical Electrical and Thermal Characteristics (Curves)

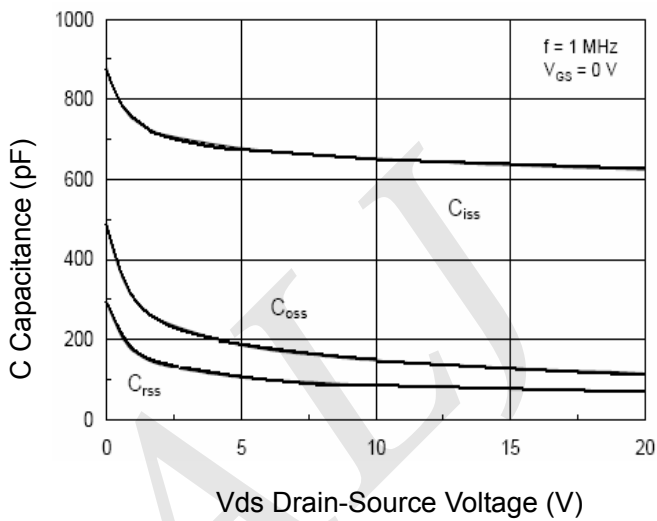


Figure 7 Capacitance vs  $V_{ds}$

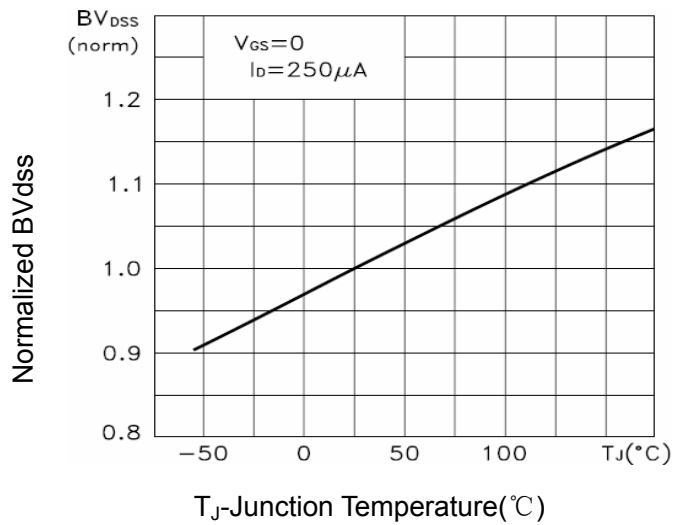


Figure 9  $BV_{DSS}$  vs Junction Temperature

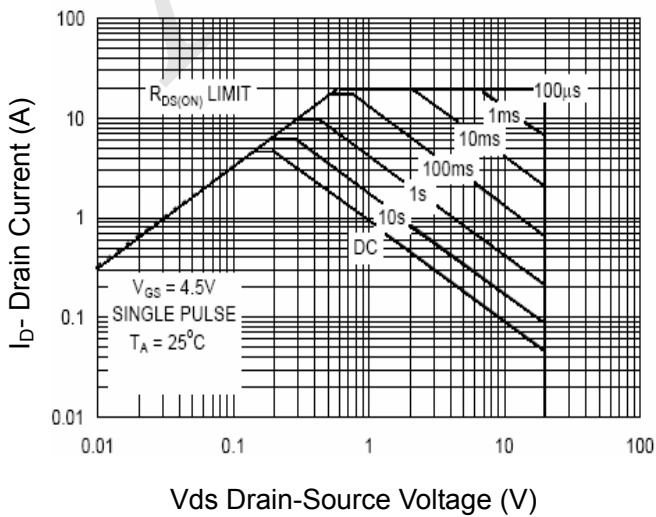


Figure 8 Safe Operation Area

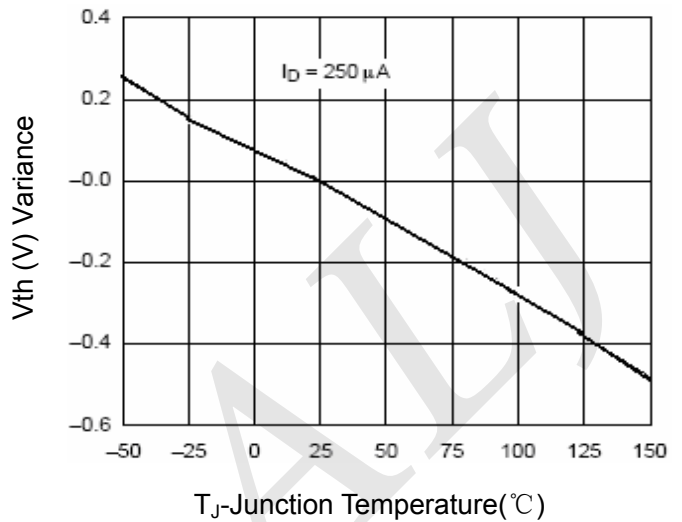


Figure 10  $V_{GS(th)}$  vs Junction Temperature

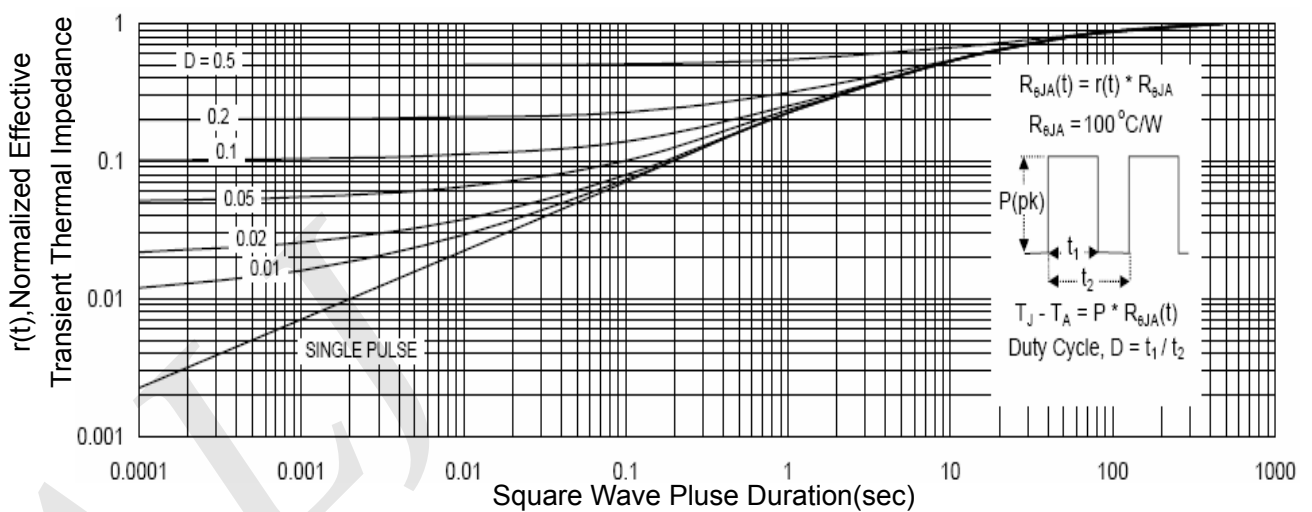


Figure 11 Normalized Maximum Transient Thermal Impedance