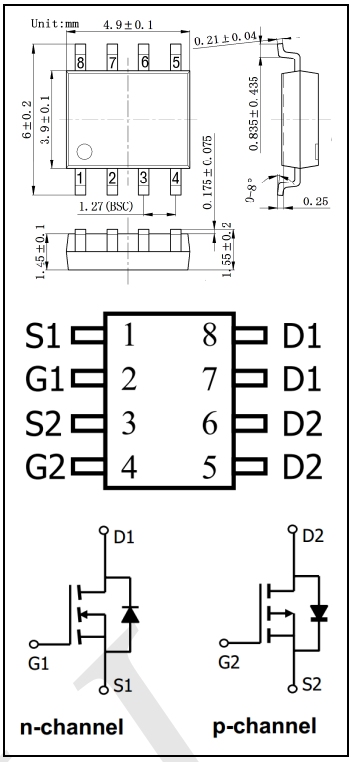
# SOP-8L Plastic-Encapsulate MOSFETS

## AO4622

Complementary Enhancement Mode Field Effect Transistor




### Features

| | n-channel | p-channel |
|---|---|---|
| ■ $V_{DS}$ (V) = | 20V | -20V |
| ■ $I_D$ = 7.3A ($V_{GS}$=4.5V) | | -5A ($V_{GS}$=-4.5V) |
| ■ $R_{DS(ON)}$ | | $R_{DS(ON)}$ |
| | < 23mΩ ($V_{GS}$=10V) | < 53mΩ ($V_{GS}$ = -4.5V) |
| | < 30mΩ ($V_{GS}$=4.5V) | < 87mΩ ($V_{GS}$ = -2.5V) |
| | < 84mΩ ($V_{GS}$=2.5V) | |

### Marking: B86

### Applications

The AO4622 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications. Standard product AO4622 is Pb-free.

### Maximum Ratings ($T_a$=25°C unless otherwise specified)

| Symbol | Parameter | | Value | | Unit |
|---|---|---|---|---|---|
| | | | N-channel | P-channel | |
| $V_{DS}$ | Drain-Source voltage | | 20 | -20 | V |
| $V_{GS}$ | Gate-Source voltage | | ±16 | ±12 | |
| $I_D$ | Continuous Drain Current [1, 6] | $T_A$ = 25 °C | 7.3 | -5 | A |
| | | $T_A$ = 70 °C | 6.2 | -4.2 | |
| $I_{DM}$ | Pulsed Drain Current [2] | | 35 | -25 | |
| $P_D$ | Power Dissipation | $T_A$ = 25 °C | 2 | 2 | W |
| | | $T_A$ = 70 °C | 1.44 | 1.44 | |
| $I_{AR}$ | Repetitive Avalanche Current [2] | | 13 | 13 | A |
| $E_{AR}$ | Repetitive Avalanche Energy 0.1mH [2] | | 25 | 25 | mJ |
| $T_j$, $T_{stg}$ | Operating Junction and Storage Temperature Range | | -55 to +150 | | °C |

### Thermal Characteristics

| Symbol | Parameter | | Device | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $R_{\theta JA}$ | Maximum Junction-to-Ambient [1] | t ≤ 10s | N-ch | 48 | 62.5 | °C/W |
| | Maximum Junction-to-Ambient [1] | Steady-State | N-ch | 74 | 110 | |
| $R_{\theta JL}$ | Maximum Junction-to-Lead [3] | Steady-State | N-ch | 35 | 40 | |
| $R_{\theta JA}$ | Maximum Junction-to-Ambient [1] | t ≤ 10s | P-ch | 48 | 62.5 | °C/W |
| | Maximum Junction-to-Ambient [1] | Steady-State | P-ch | 74 | 110 | |
| $R_{\theta JL}$ | Maximum Junction-to-Lead [3] | Steady-State | P-ch | 35 | 40 | |

## N-Channel Electrical Characteristics ($T_J$=25°C unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0V, $I_D$ = 250μA | 20 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 16V, $V_{GS}$ = 0V | | | 1 | μA |
| | | $V_{DS}$ = 16V, $V_{GS}$=0V, $T_J$= 55°C | | | 5 | |
| $I_{GSS}$ | Gate-body Leakage current | $V_{DS}$ = 0V, $V_{GS}$ = ±16V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate-Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA | 0.6 | 1.25 | 2 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}$ = 4.5V, $V_{DS}$ = 5V | 35 | | | A |
| $R_{DS(on)}$ | Drain-Source On-Resistance | $V_{GS}$ = 10V, $I_D$ = 7.3A | | 19 | 23 | mΩ |
| | | $V_{GS}$ = 10V, $I_D$ = 7.3A, $T_J$ = 55°C | | 28 | 33.6 | |
| | | $V_{GS}$ = 4.5V, $I_D$ = 6.4A | | 24 | 30 | |
| | | $V_{GS}$ = 2.5V, $I_D$ = 4.5A | | 67 | 84 | |
| $g_{fs}$ | Forward Trans conductance | $V_{DS}$ = 5V, $I_D$ =7.3A | | 17 | | S |
| $I_S$ | Maximum Body-Diode Continuous Current | | | | 3 | A |
| $V_{SD}$ | Diode Forward Voltage | $I_S$ = 1A | | 0.7 | 1 | V |
| **Dynamic** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$ = 0V<br>$V_{DS}$ = 10V<br>f = 1.0MHz | | 900 | 1100 | pF |
| $C_{oss}$ | Output Capacitance | | | 162 | | |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 105 | | |
| $R_g$ | Gate resistance | $V_{GS}$ = 0V, $V_{DS}$ = 0V, f = 1MHz | | 1.8 | 2.7 | Ω |
| **Switching** | | | | | | |
| $Q_g$(10V) | Total Gate Charge | $V_{GS}$ = 10V,<br>$I_D$ = 10A,<br>$V_{DS}$ = 6.5V | | 15 | 18 | nC |
| $Q_g$(4.5V) | Total Gate Charge | | | 7.2 | 9 | |
| $Q_{gs}$ | Gate-Source Charge | | | 1.8 | | |
| $Q_{gd}$ | Gate-Drain Charge | | | 2.8 | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{GS}$ = 10V, $V_{DS}$ = 10V, $R_L$=1.4Ω,<br>$R_{GEN}$ = 3Ω | | 4.5 | | ns |
| $t_r$ | Rise Time | | | 9.2 | | |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 18.7 | | |
| $t_f$ | Fall Time | | | 3.3 | | |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$ = 7.3A, dI/dt = 100A/μs | | 18 | | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | | | 9.5 | | nC |

**Notes**

1. The value of $R_{\theta JA}$ is measured with the device mounted on 1in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$ = 25°C. The value in any given application depends on the user's specific board design.
2. Repetitive rating, pulse width limited by junction temperature.
3. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient. $R_{\theta JL}$ and $R_{\theta JC}$ are equivalent terms referring to thermal resistance from junction to drain lead.
4. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.
5. These tests are performed with the device mounted on 1 in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25°C. The SOA curve provides a single pulse rating.
6. The current rating is based on the t ≤ 10s thermal resistance rating.

## N-Channel Typical Characteristics

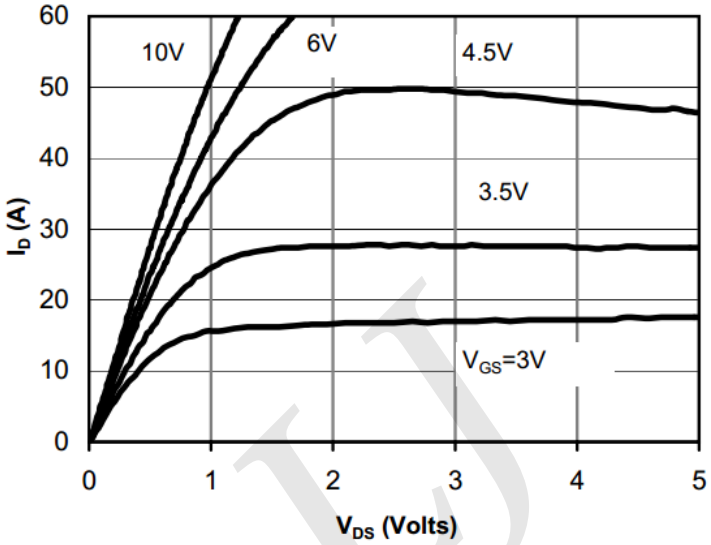



Figure 1: On-Region Characteristics

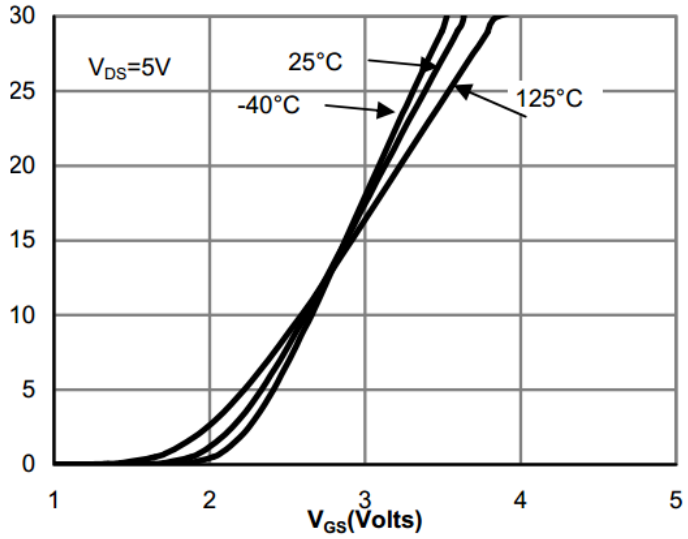



Figure 2: Transfer Characteristics

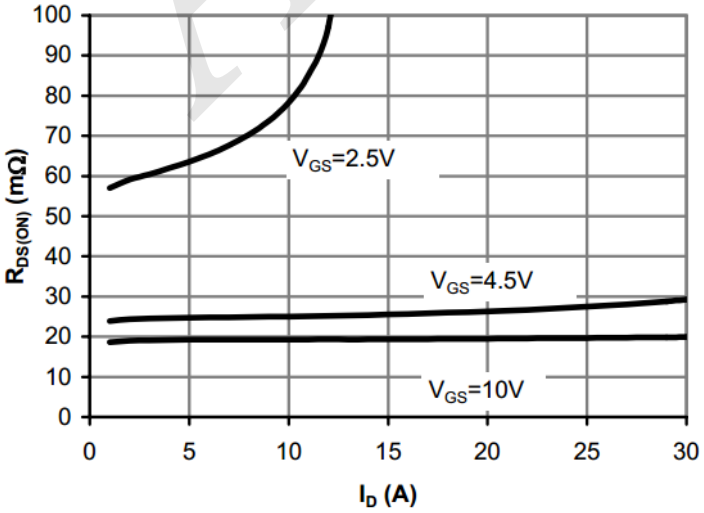



Figure 3: On-Resistance vs. Drain Current and Gate Voltage

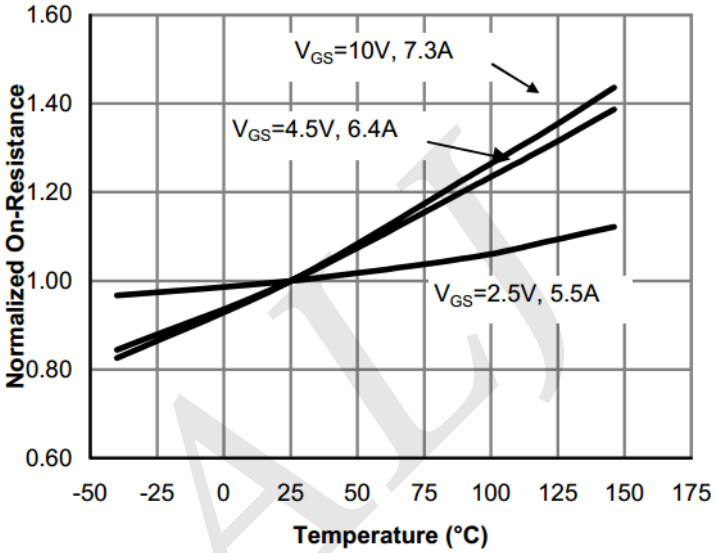



Figure 4: On-Resistance vs. Junction Temperature

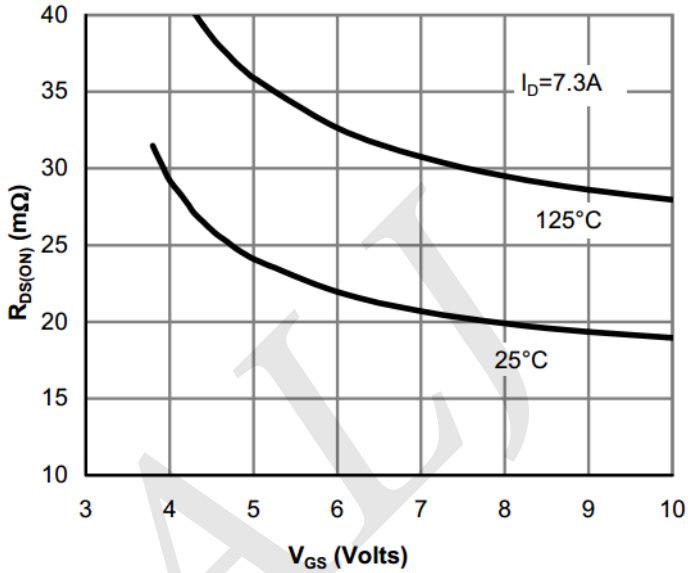



Figure 5: On-Resistance vs. Gate-Source Voltage

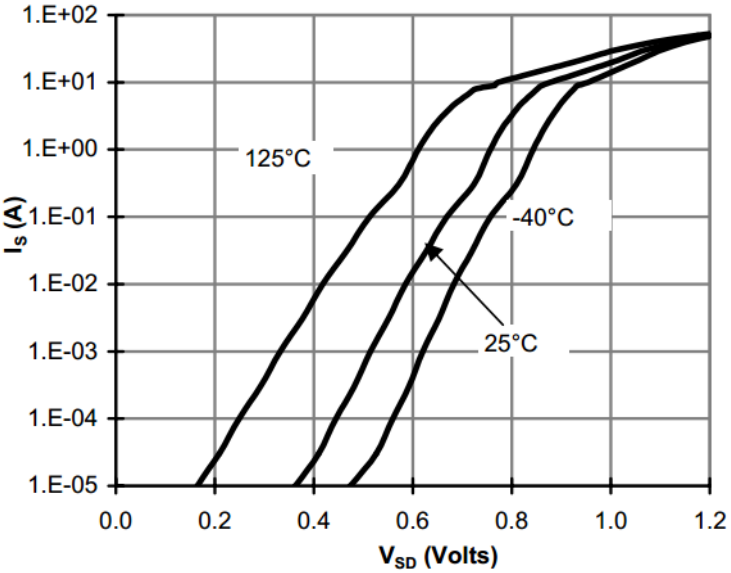



Figure 6: Body-Diode Characteristics

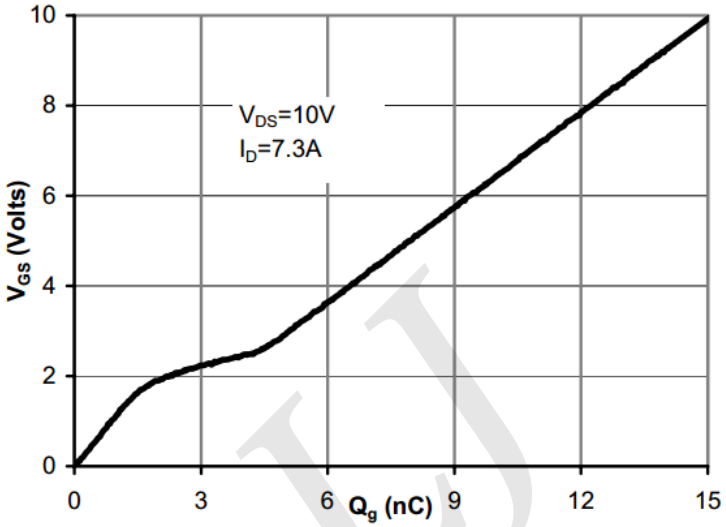



Figure 7: Gate-Charge Characteristics

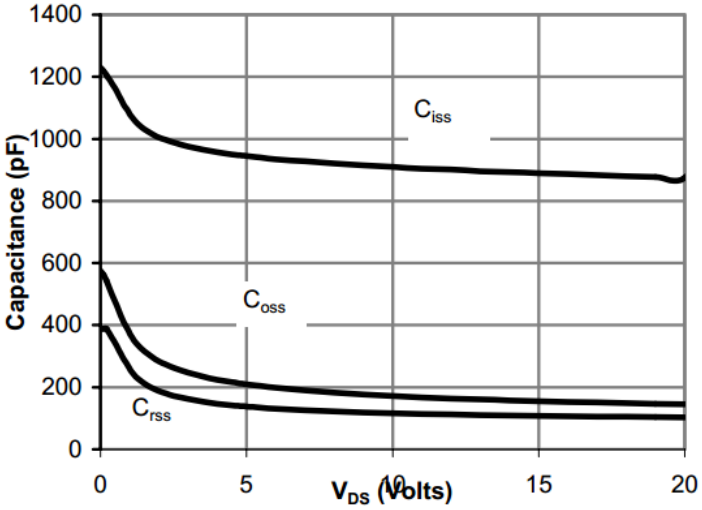



Figure 8: Capacitance Characteristics

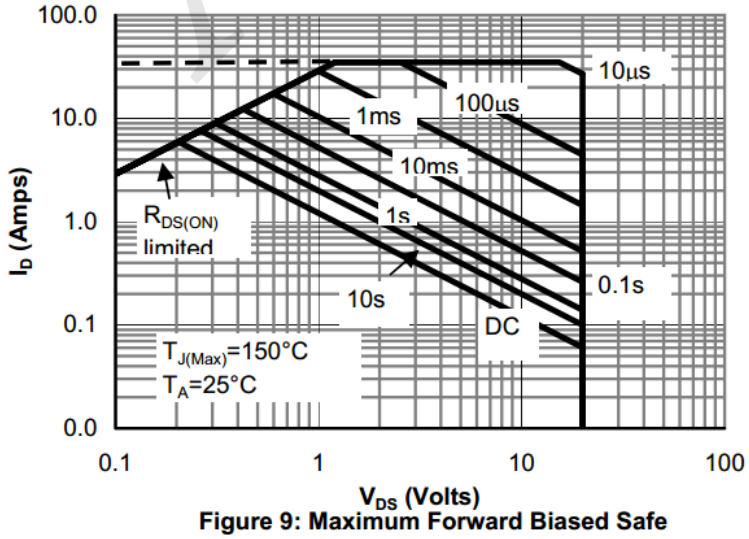



Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

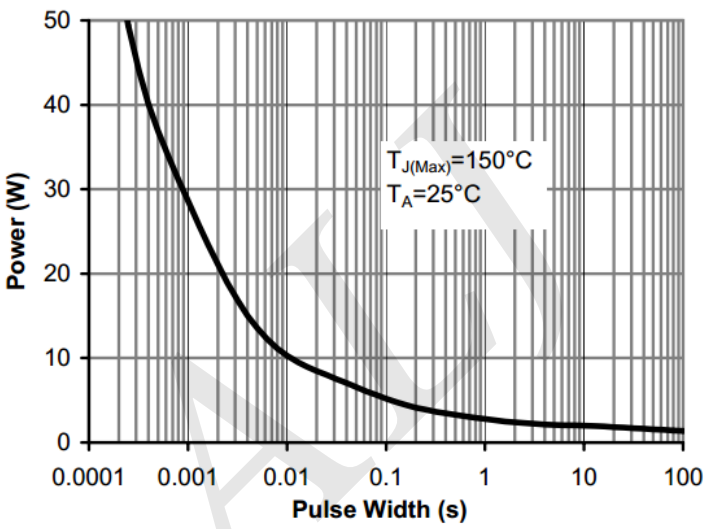



Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

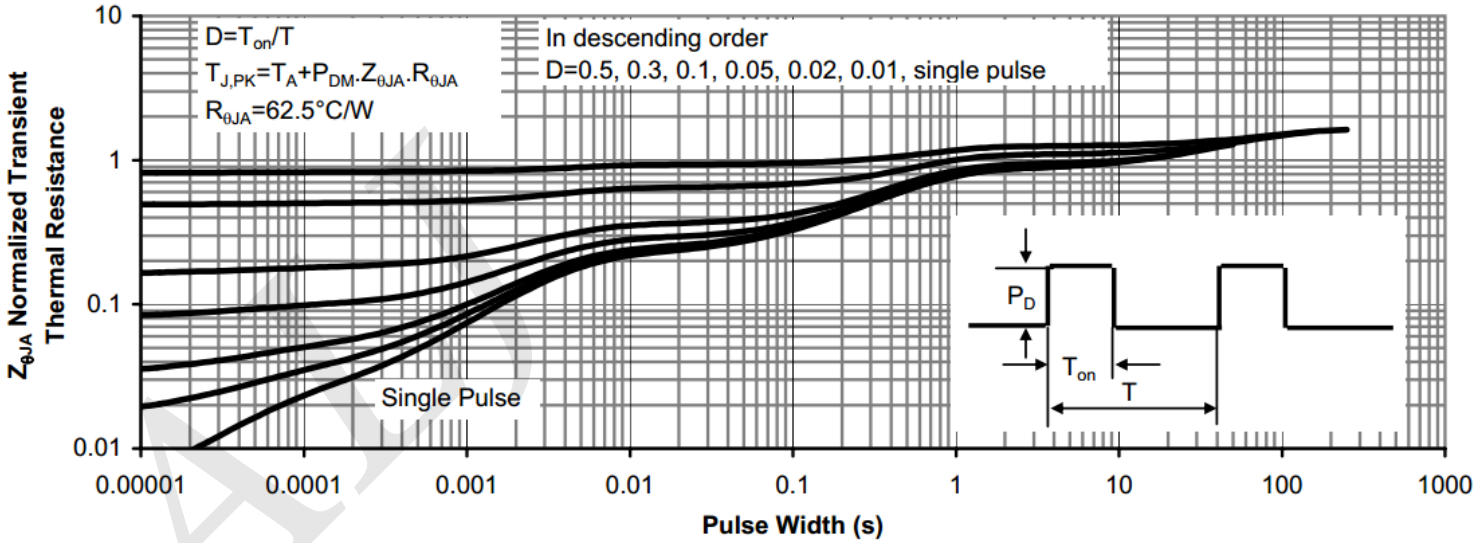



Figure 11: Normalized Maximum Transient Thermal Impedance

## P-Channel Electrical Characteristics ($T_J$=25°C unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0V, $I_D$ = -250μA | -20 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = -16V, $V_{GS}$ = 0V | | | -1 | μA |
| | | $V_{DS}$ = -16V, $V_{GS}$=0V, $T_J$= 55°C | | | -5 | |
| $I_{GSS}$ | Gate-body Leakage current | $V_{DS}$ = 0V, $V_{GS}$ = ±12V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate-Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = -250μA | -1.3 | -0.9 | -0.5 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}$ = -4.5V, $V_{DS}$ = -5V | -25 | | | A |
| $R_{DS(on)}$ | Drain-Source On-Resistance | $V_{GS}$ = -4.5V, $I_D$ = -5A | | 44 | 53 | mΩ |
| | | $V_{GS}$ = -4.5V, $I_D$ = -5A, $T_J$ = 125°C | | 59 | 71 | |
| | | $V_{GS}$ = -2.5V, $I_D$ = -4.2A | | 67 | 87 | |
| $g_{fs}$ | Forward Trans conductance | $V_{DS}$ = -5V, $I_D$ =-5A | | 13 | | S |
| $I_S$ | Maximum Body-Diode Continuous Current | | | | -2.5 | A |
| $V_{SD}$ | Diode Forward Voltage | $I_S$ = -1A, $V_{GS}$ = 0V | | -0.76 | -1 | V |
| **Dynamic** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$ = 0V<br>$V_{DS}$ = -10V<br>f = 1.0MHz | | 800 | 960 | pF |
| $C_{oss}$ | Output Capacitance | | | 131 | | |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 103 | | |
| $R_g$ | Gate resistance | $V_{GS}$ = 0V, $V_{DS}$ = 0V, f = 1MHz | | 6.7 | 10 | Ω |
| **Switching** | | | | | | |
| $Q_g$(10V) | Total Gate Charge | $V_{GS}$ = -4.5V,<br>$I_D$ = -4.5A,<br>$V_{DS}$ = -10V | | 15.5 | | nC |
| $Q_g$(4.5V) | Total Gate Charge | | | 7.4 | | |
| $Q_{gs}$ | Gate-Source Charge | | | 1.3 | | |
| $Q_{gd}$ | Gate-Drain Charge | | | 2.9 | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{GS}$ = -4.5V, $V_{DS}$ = -10V, $R_L$=2Ω,<br>$R_{GEN}$ = 3Ω | | 4.4 | | ns |
| $t_r$ | Rise Time | | | 7.6 | | |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 44 | | |
| $t_f$ | Fall Time | | | 13.5 | | |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$ = -5A, dI/dt = 100A/μs | | 20 | | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | | | 9 | | nC |

**Notes**

1. The value of $R_{\theta JA}$ is measured with the device mounted on 1in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$ = 25°C. The value in any given application depends on the user's specific board design.
2. Repetitive rating, pulse width limited by junction temperature.
3. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient. $R_{\theta JL}$ and $R_{\theta JC}$ are equivalent terms referring to thermal resistance from junction to drain lead.
4. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.
5. These tests are performed with the device mounted on 1 in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25°C. The SOA curve provides a single pulse rating.
6. The current rating is based on the t ≤ 10s thermal resistance rating.

## P-Channel Typical Characteristics

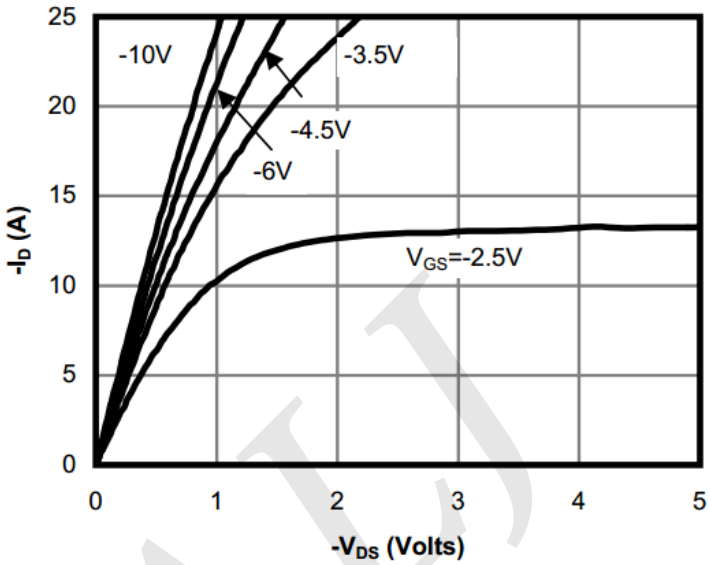



Fig 1: On-Region Characteristics

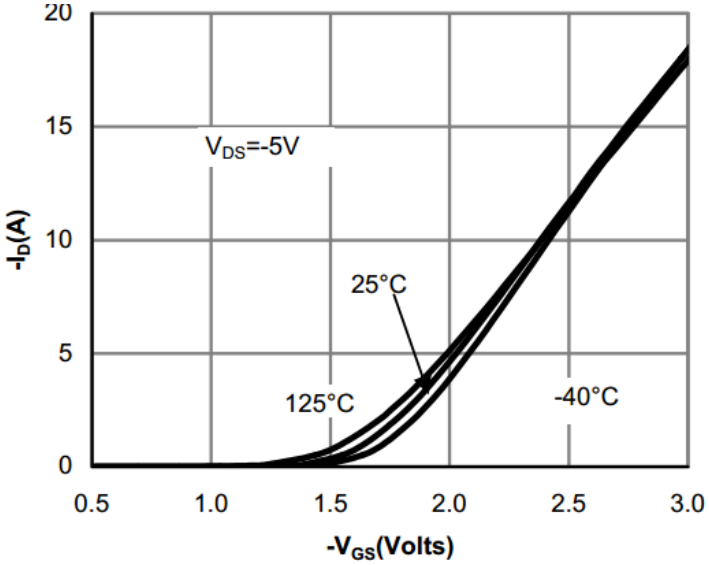



Figure 2: Transfer Characteristics

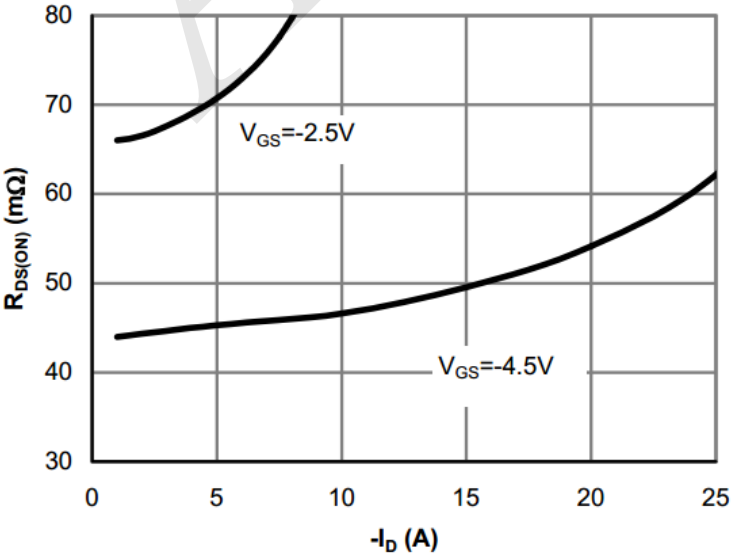



Figure 3: On-Resistance vs. Drain Current and Gate Voltage

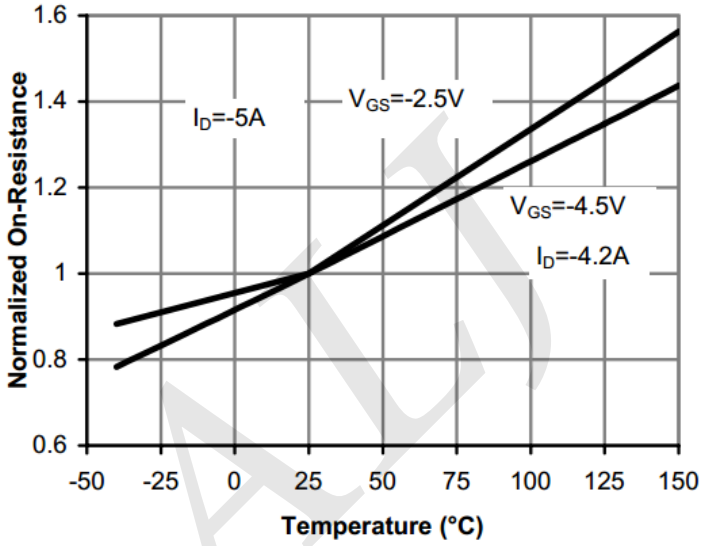



Figure 4: On-Resistance vs. Junction Temperature

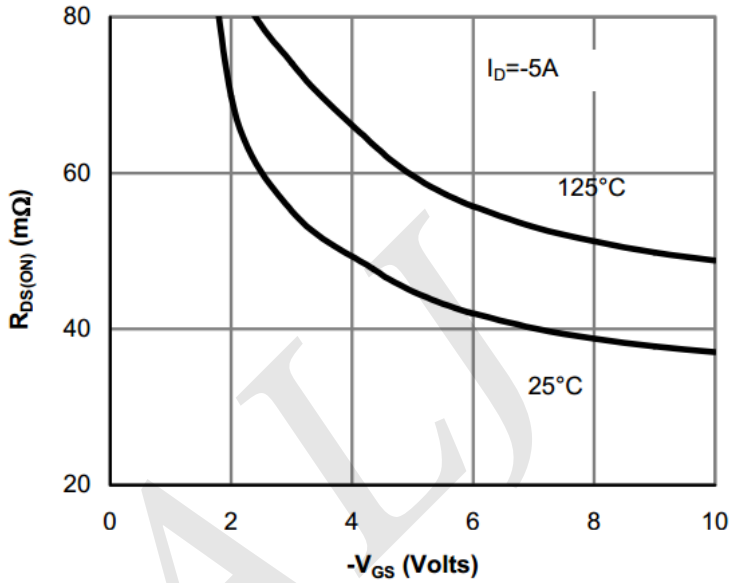



Figure 5: On-Resistance vs. Gate-Source Voltage

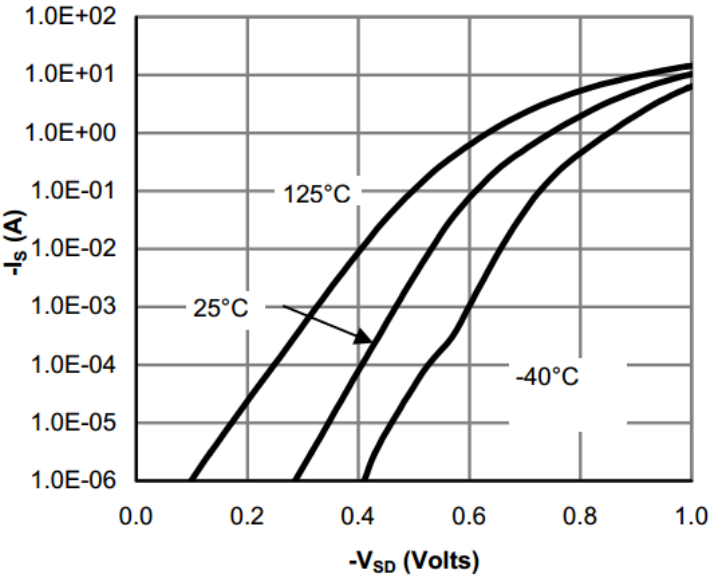



Figure 6: Body-Diode Characteristics

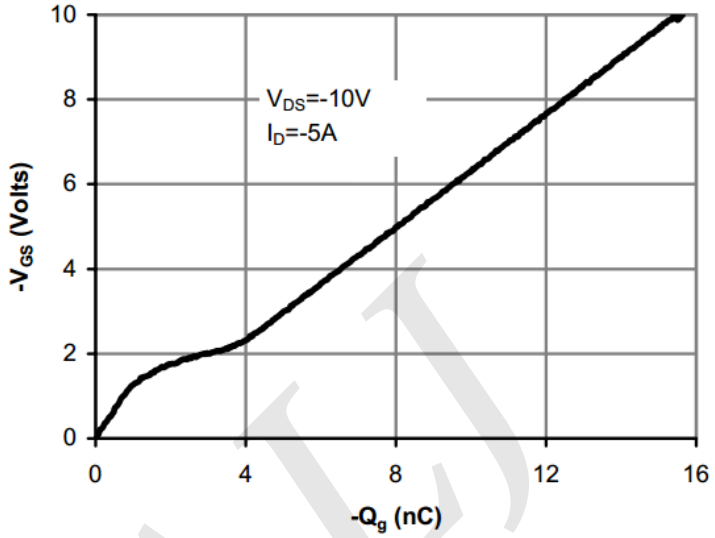



Figure 7: Gate-Charge Characteristics

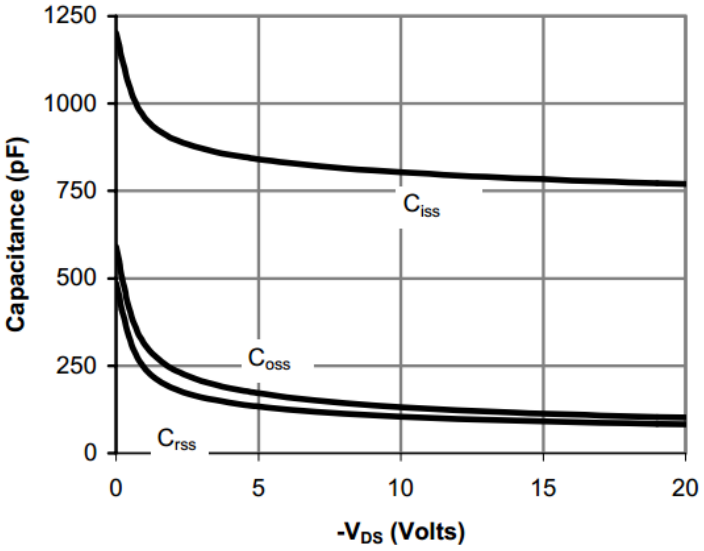



Figure 8: Capacitance Characteristics

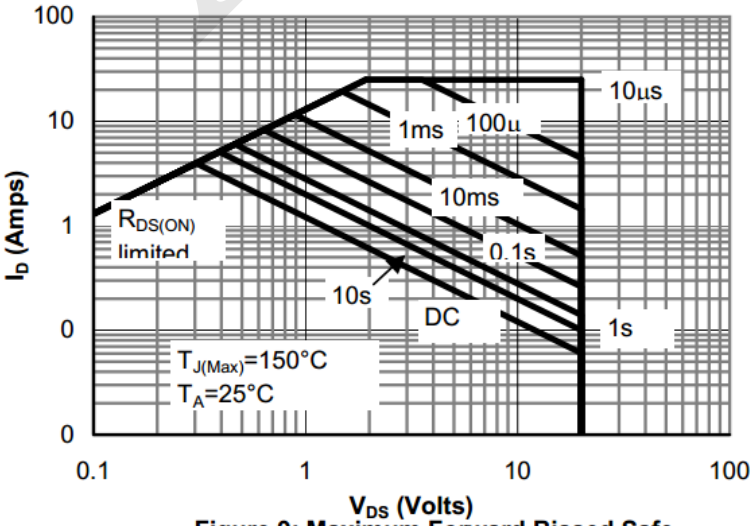



Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

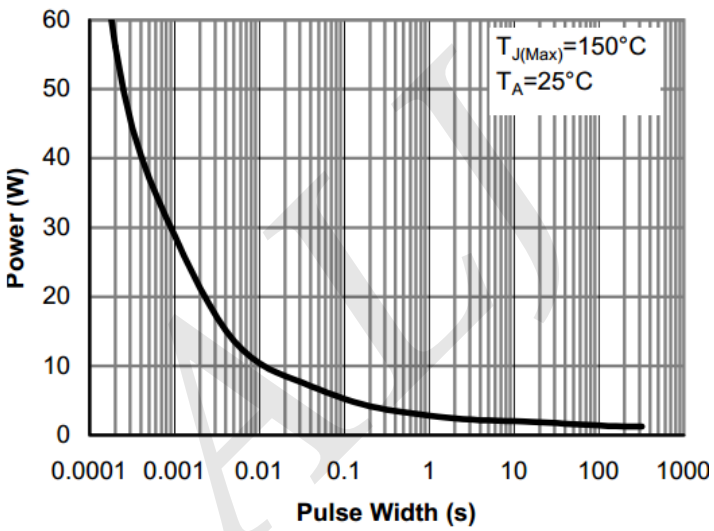



Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

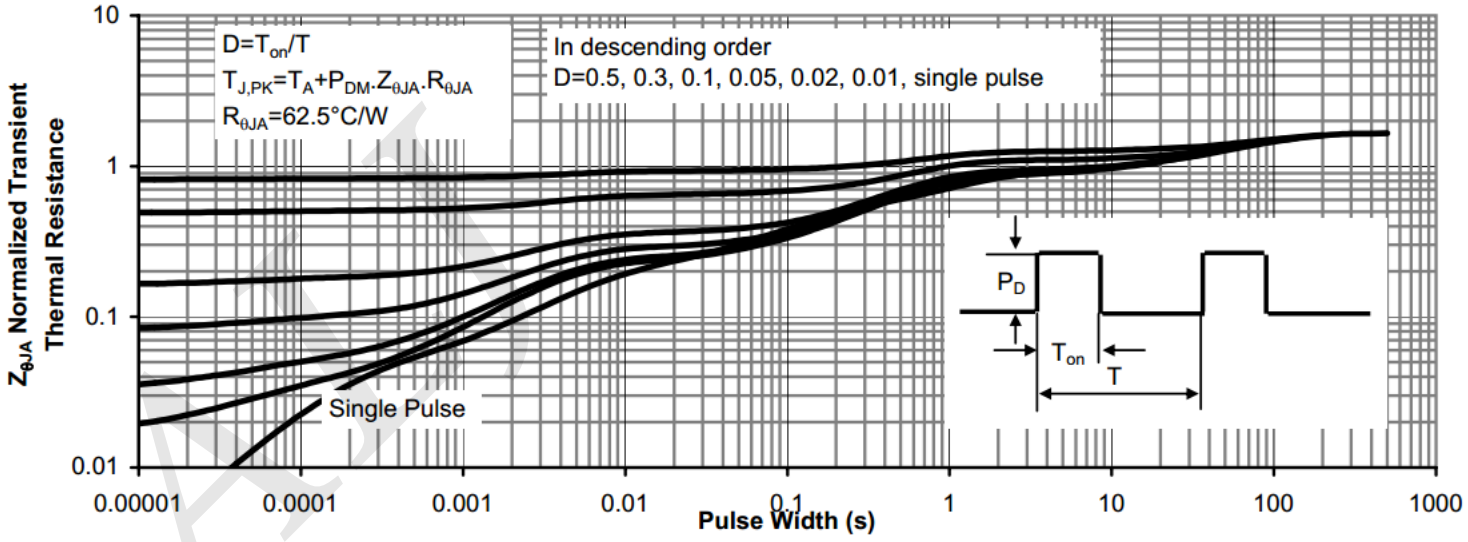



Figure 11: Normalized Maximum Transient Thermal Impedance