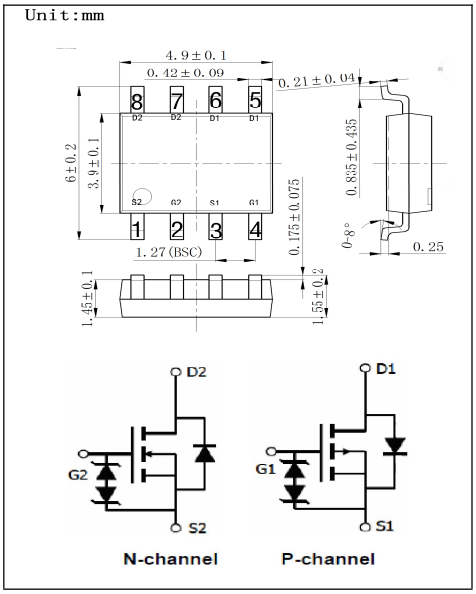
# SOP-8L Plastic-Encapsulate MOSFETS

## LJ4525

N and P-Channel Enhancement Mode Power MOSFET




### Features

- N-Channel: $V_{DS}$ = 40V, $I_D$ = 7A, $R_{DS(ON)}$ < 24mΩ @ $V_{GS}$ = 10V
  $R_{DS(ON)}$ < 38mΩ @ $V_{GS}$ = 4.5V
- P-Channel:$V_{DS}$ = -40V, $I_D$ = -5A $R_{DS(ON)}$ < 38mΩ @ $V_{GS}$ = -10V
  $R_{DS(ON)}$ < 50mΩ @ $V_{GS}$ = -4.5V
- High power and current handing capability
- Lead free product is acquired
- Surface mount package

**Marking**: A55

### Description

The NCE4525 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOS -FETS may be used to form a level shifted high side switch,and for a host of other applications.

### Absolute Maximum Ratings

| Symbol | Parameter | N-Channel | P-Channel | Unit |
|---|---|---|---|---|
| $V_{DS}$ | Drain Current Voltage | 40 | -40 | V |
| $V_{GS}$ | Gate-Source Voltage | ±12 | ±12 | V |
| $I_D$ | Continuous Drain Current $T_A$ = 25°C | 7 | -5 | A |
| | Continuous Drain Current $T_A$ = 70°C | 5.8 | -4.2 | |
| $I_{DM}$ | Pulsed Drain Current [1)] | 30 | -30 | A |
| $P_D$ | Maximum Power Dissipation $T_A$ = 25°C | 2.0 | 2.0 | W |
| $T_J$, $T_{STG}$ | Operating Junction and Storage Temperature Range | -55 to + 150 | -55 to + 150 | °C |

### Thermal Resistance

| Symbol | Parameter | | Max | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-Ambient (Note 2) | N-Ch | 62.5 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient(Note 2) | P-Ch | 62.5 | |

## N-CH Electrical Characteristics ($T_J$=25°C unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source breakdown voltage | $V_{GS}$ = 0V, $I_D$ = 250μA | 40 | | | V |
| $I_{DSS}$ | Drain-to-Source leakage current | $V_{DS}$ = 40V, $V_{GS}$ = 0V | | | 1 | μA |
| $I_{GSS}$ | Gate-to-Source forward leakage | $V_{GS}$ = ±10V, $V_{DS}$ = 0V | | | ±10 | μA |
| $V_{GS(th)}$ | Gate threshold voltage(Note 3) | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA | 1 | 1.5 | 2 | V |
| $R_{DS(on)}$ | Static drain-to-source on-resistance(Note 3) | $V_{GS}$ = 10V, $I_D$ = 6A | | 19.5 | 24 | mΩ |
| | | $V_{GS}$ = 4.5V, $I_D$ = 5A | | 29 | 38 | |
| $g_{fs}$ | Forward Trans conductance(Note 3) | $V_{DS}$ = 5V, $I_D$ = 6A | 15 | | | S |
| $Q_g$ | Total Gate Charge(Note 4) | $V_{DS}$ = 20V, $I_D$ = 6A, $V_{GS}$ = 10V | | 8.9 | | nC |
| $Q_{gs}$ | Gate-to-Source Charge | | | 2.4 | | |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | | | 1.4 | | |
| $t_{d(on)}$ | Turn-On Delay Time(Note 4) | $V_{DD}$ = 15V, $R_L$ = 2.5Ω, $V_{GS}$ = 10V, $R_{GEN}$ = 3Ω | | 4.5 | | nS |
| $t_r$ | Rise Time | | | 2.5 | | |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 14.5 | | |
| $t_f$ | Fall Time | | | 3.5 | | |
| $C_{iss}$ | Input Capacitance(Note 4) | $V_{GS}$ = 0V, $V_{DS}$ = 20V, $f$ = 1.0MHz | | 516 | | pF |
| $C_{oss}$ | Output Capacitance | | | 82 | | |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 43 | | |
| $V_{SD}$ | Diode Forward Voltage(Note 3) | $V_{GS}$ = 0V, $I_S$ = 6A | | 0.8 | 1.2 | V |

## P-CH Electrical Characteristics ($T_J$=25°C unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source breakdown voltage | $V_{GS}$ = 0V, $I_D$ = -250μA | -40 | | | V |
| $I_{DSS}$ | Drain-to-Source leakage current | $V_{DS}$ = -40V, $V_{GS}$ = 0V | | | -1 | μA |
| $I_{GSS}$ | Gate-to-Source forward leakage(Note 3) | $V_{GS}$ = ±10V, $V_{DS}$ = 0V | | | ±10 | μA |
| $V_{GS(th)}$ | Gate threshold voltage(Note 3) | $V_{DS}$ = $V_{GS}$, $I_D$ = -250μA | -1 | -1.5 | -2 | V |
| $R_{DS(on)}$ | Static drain-to-source on-resistance(Note 3) | $V_{GS}$ = -10V, $I_D$ = -5A | | 32 | 38 | mΩ |
| | | $V_{GS}$ = -4.5V, $I_D$ = -4A | | 39 | 50 | |
| $g_{fs}$ | Forward Trans conductance | $V_{DS}$ = -5V, $I_D$ = -5A | 10 | | | S |
| $Q_g$ | Total Gate Charge(Note 4) | $V_{DS}$ = -20V, $I_D$ = -5A, $V_{GS}$ = -10V | | 17 | | nC |
| $Q_{gs}$ | Gate-to-Source Charge | | | 3.4 | | |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | | | 3.2 | | |
| $t_{d(on)}$ | Turn-On Delay Time(Note 4) | $V_{DD}$ = -20V, $R_L$ = 2.3Ω, $V_{GS}$ = -10V, $R_{GEN}$ = 6Ω | | 6.2 | | ns |
| $t_r$ | Rise Time | | | 8.4 | | |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 44.8 | | |
| $t_f$ | Fall Time | | | 16 | | |
| $C_{iss}$ | Input Capacitance(Note 4) | $V_{GS}$ = 0V, $V_{DS}$ = -20V, $f$ = 1.0MHz | | 940 | | pF |
| $C_{oss}$ | Output Capacitance | | | 97 | | |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 72 | | |
| $V_{SD}$ | Diode Forward Voltage(Note 3) | $V_{GS}$ = 0V, $I_S$ = -5A | | | -1.2 | V |

**Note:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production.

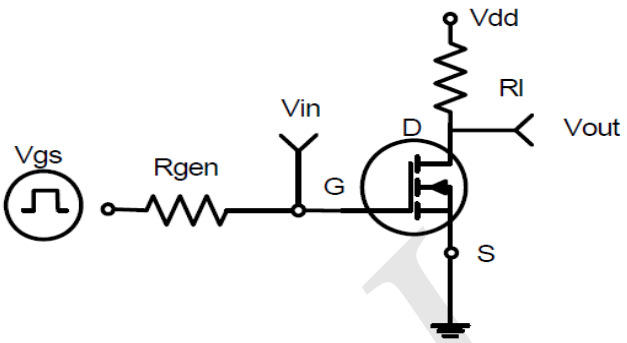



**Figure 1:Switching Test Circuit**

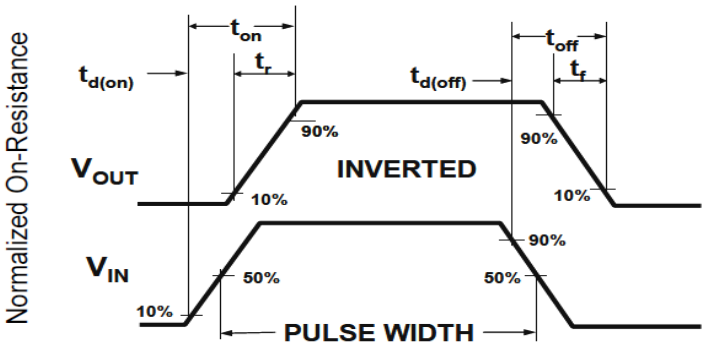



**Figure 2:Switching Waveforms**

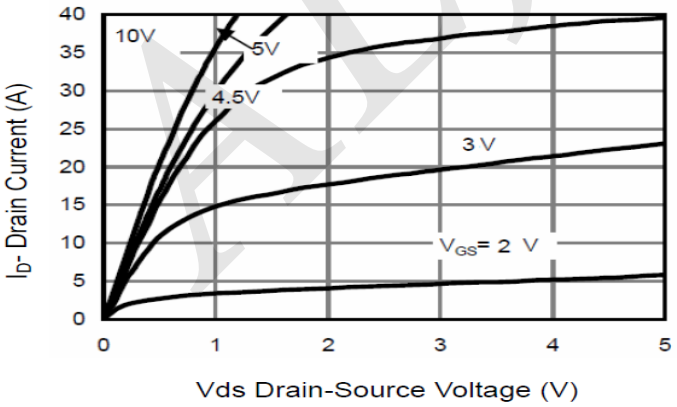



**Figure 3 Output Characteristics**

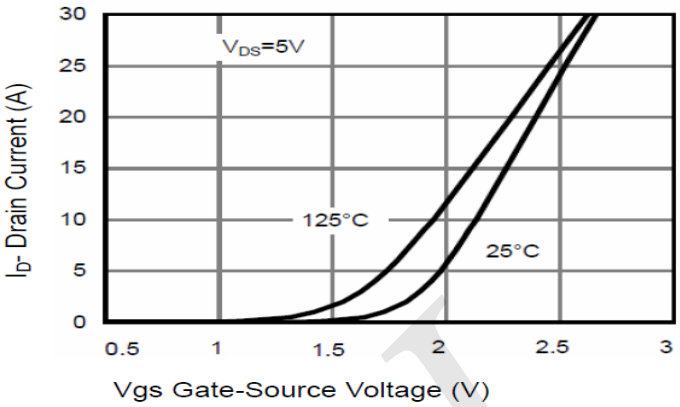



**Figure 4 Transfer Characteristics**

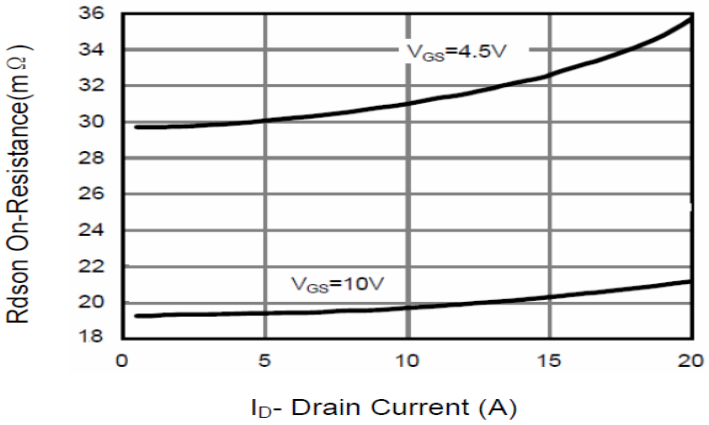



**Figure 5 Drain-Source On-Resistance**

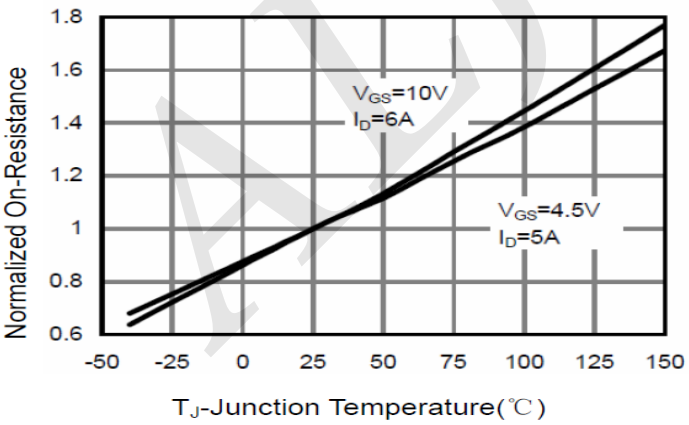



**Figure 6 Drain-Source On-Resistance**

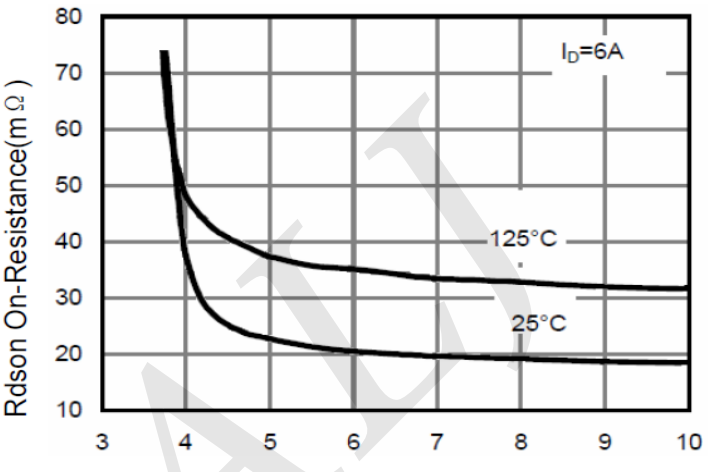



**Figure7 Rdson vs Vgs**

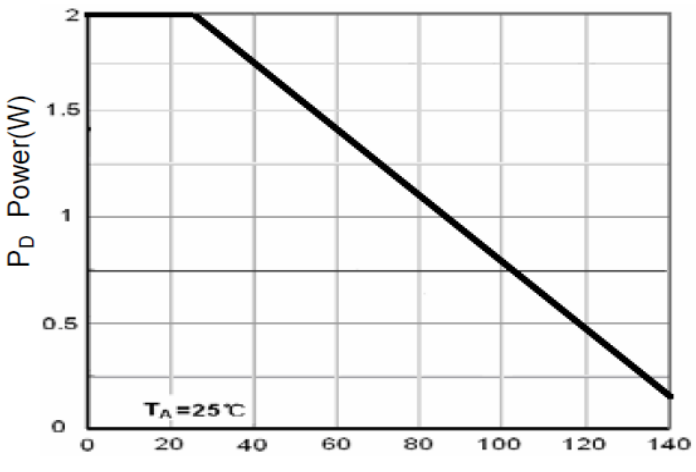



**Figure 8 Power Dissipation**

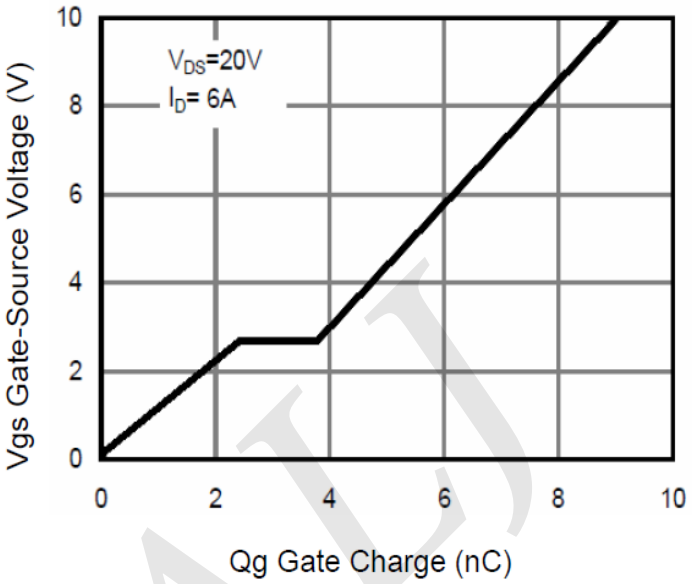



**Figure 9 Gate Charge**

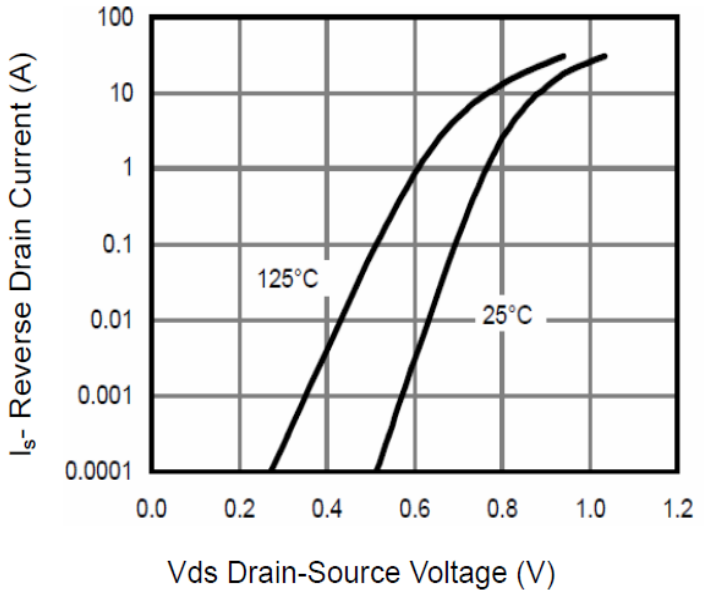



**Figure 10 Source- Drain Diode Forward**

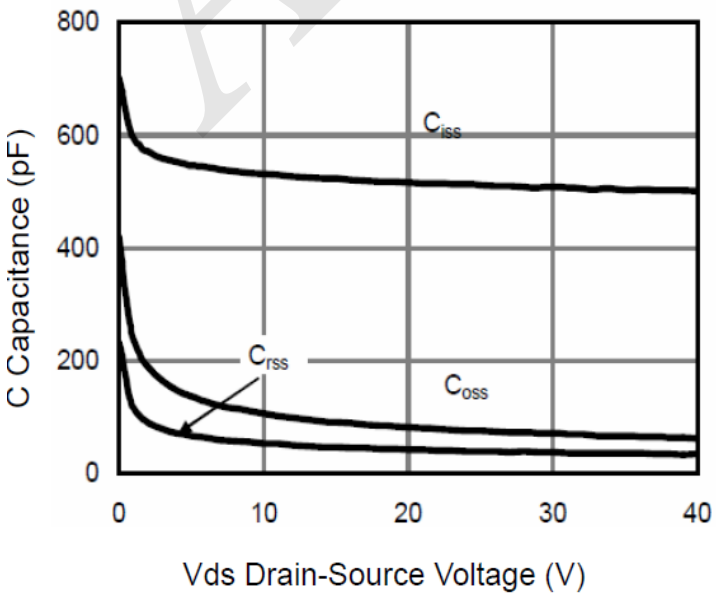



**Figure 11 Capacitance vs Vds**

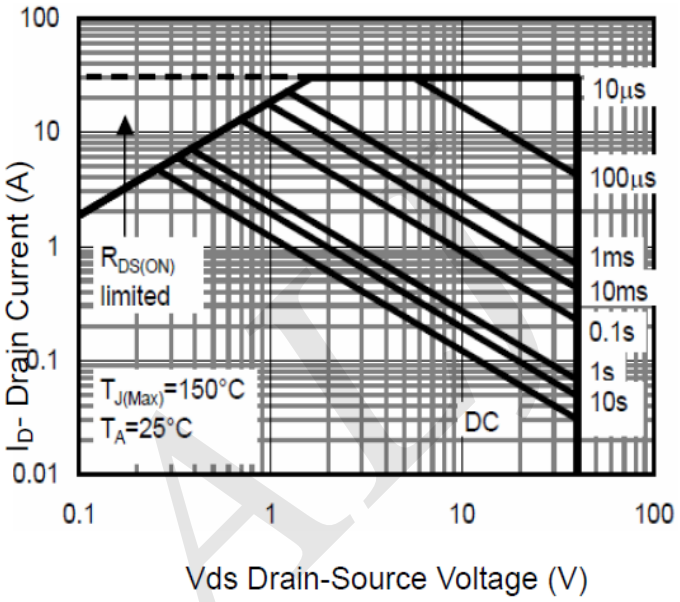



**Figure 12 Safe Operation Area**

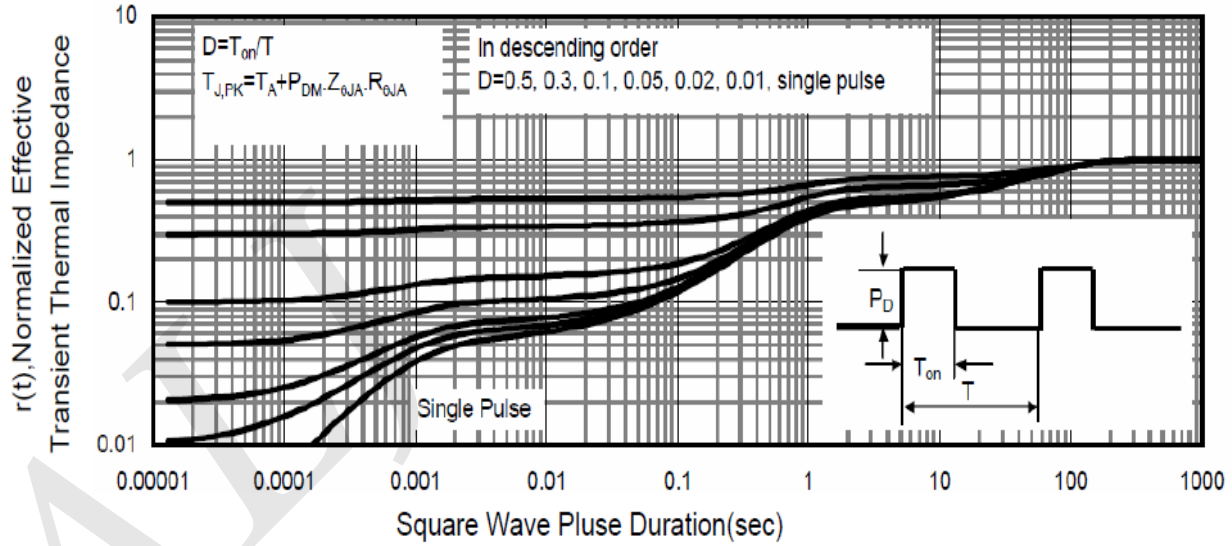



**Figure 13 Normalized Maximum Transient Thermal Impedance**

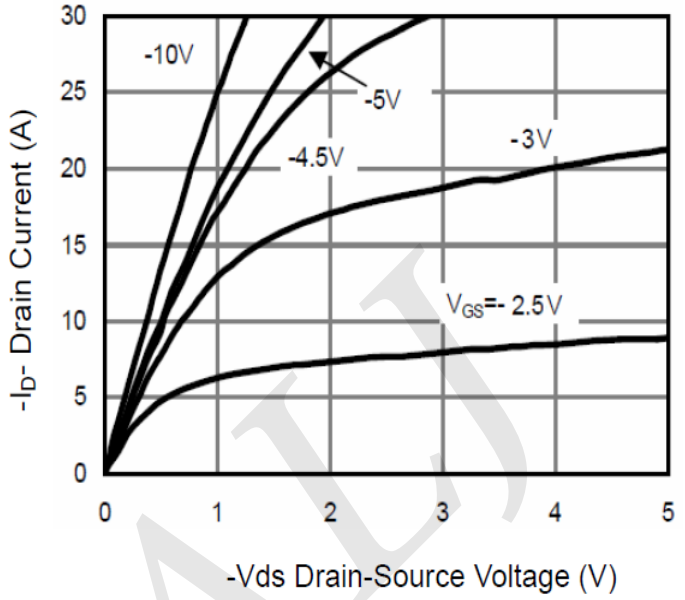



**Figure 1 Output Characteristics**

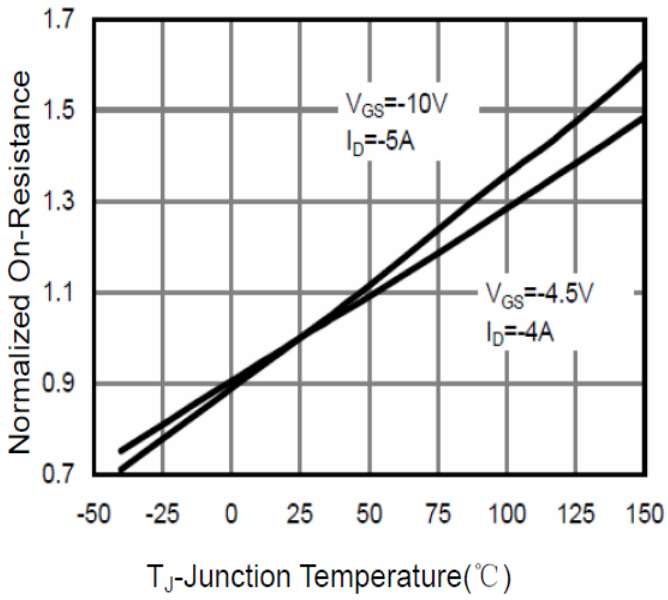



**Figure 4 Rdson-Junction Temperature**

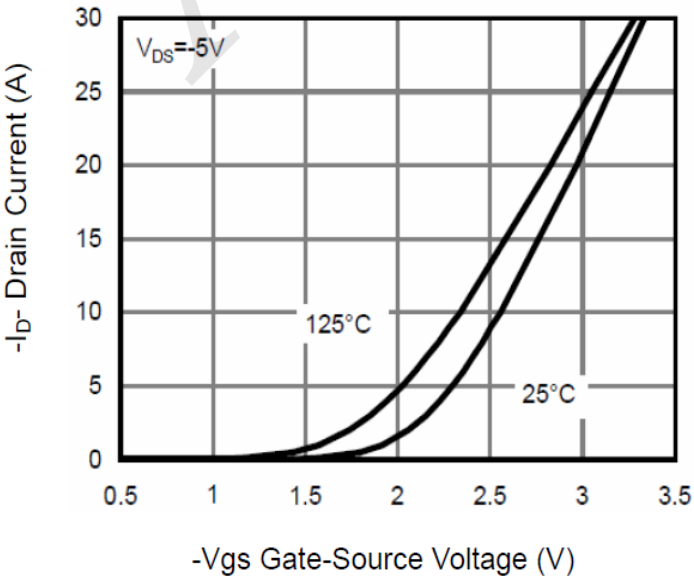



**Figure 2 Transfer Characteristics**

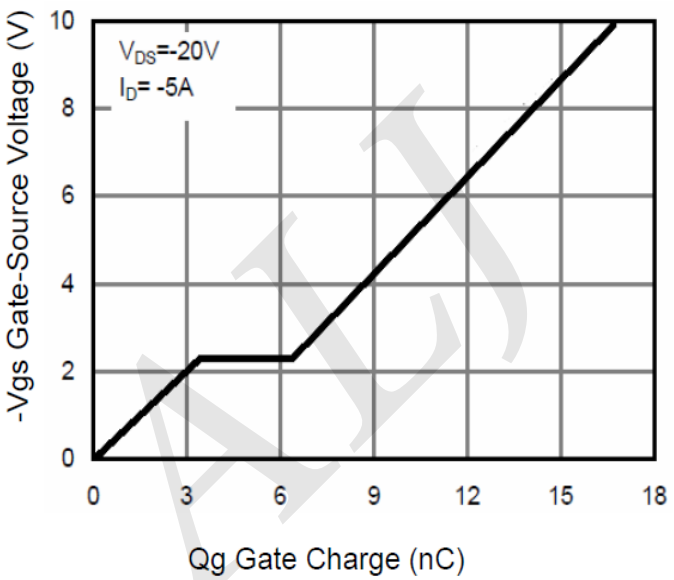



**Figure 5 Gate Charge**

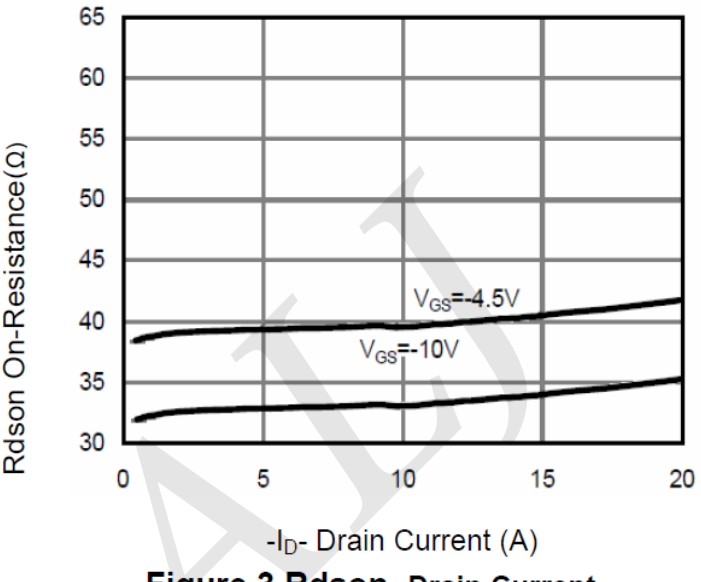



**Figure 3 Rdson- Drain Current**

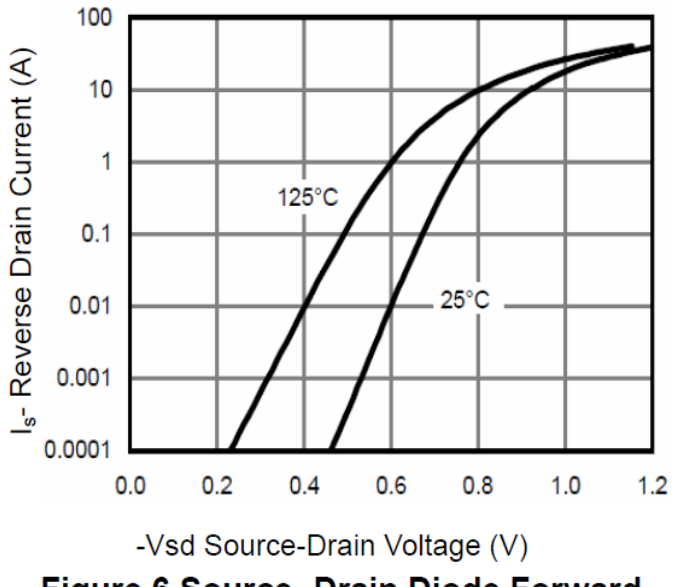



**Figure 6 Source- Drain Diode Forward**

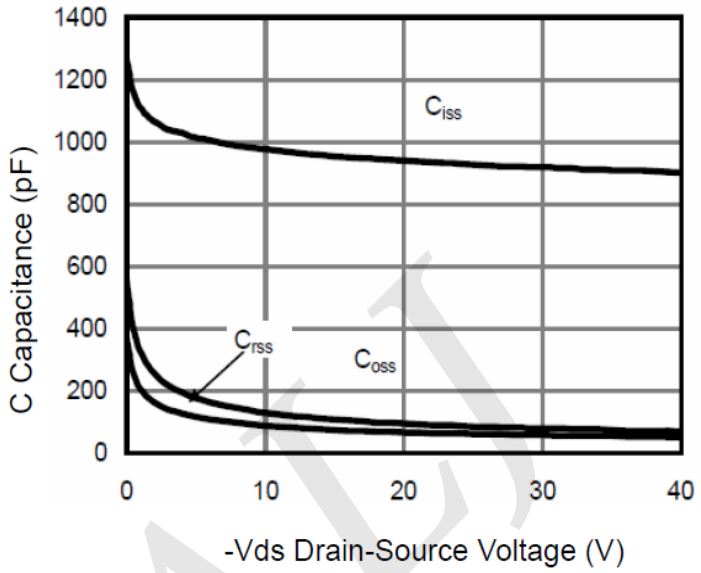



**Figure 7 Capacitance vs Vds**

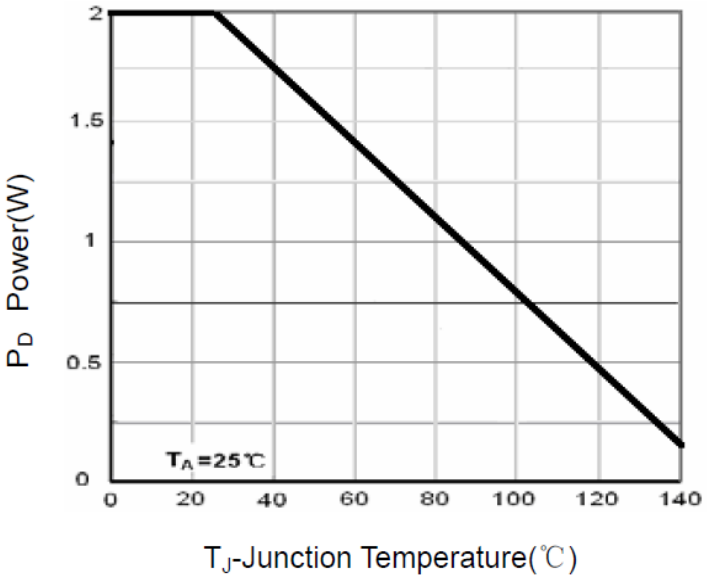



**Figure 9 Power Dissipation**

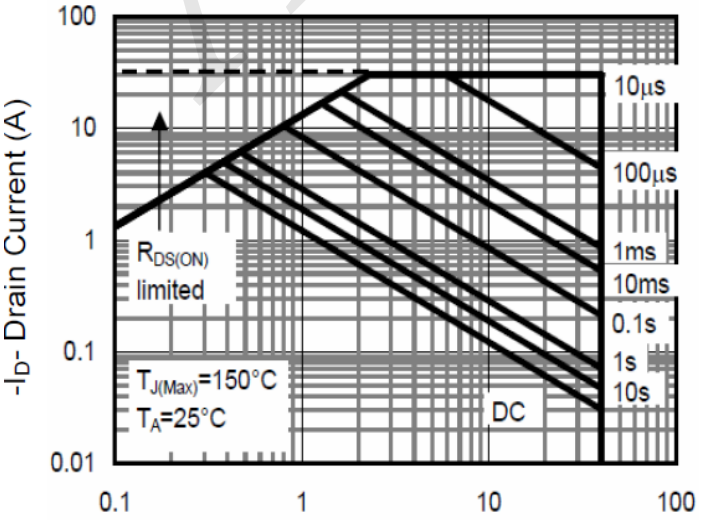



**Figure 8 Safe Operation Area**

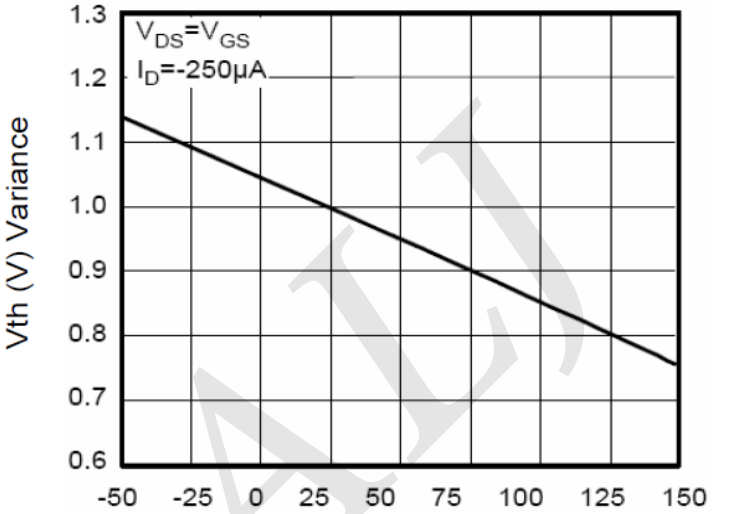



**Figure 10 $V_{GS(th)}$ vs Junction Temperature**

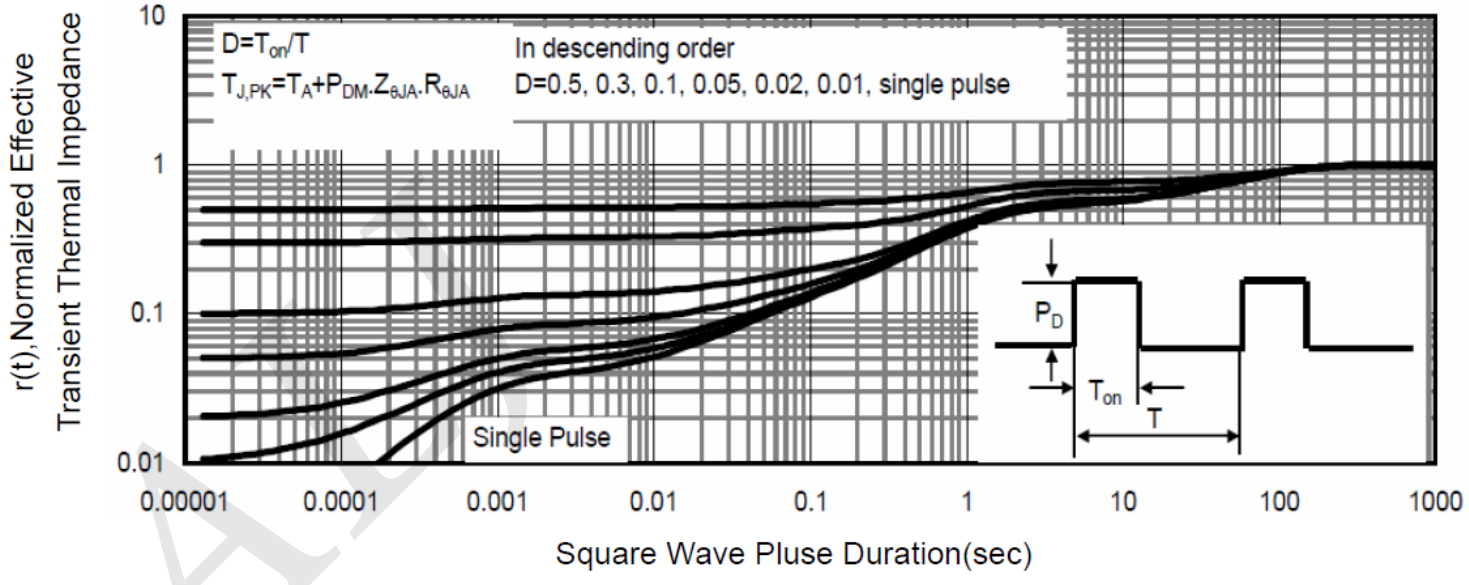



**Figure 11 Normalized Maximum Transient Thermal Impedance**